

## Fabrication of high-quality GaAs/diamond heterointerface for thermal management applications

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### ABSTRACT

The direct integrating of GaAs and diamond is achieved at room temperature via a surface activated bonding method. An ultrathin crystal defect layer composed of GaAs and diamond was formed at the bonding interface. The thickness of the GaAs and diamond crystal defect layers was determined to be 0.4 and 1.6 nm, respectively. After annealing at 400 °C, no changes were observed in the thickness of the crystal defect layer and the interfacial structure. The thermal characterization of the transmission line model (TLM) patterns formed on the GaAs layer bonded to diamond and sapphire substrates is demonstrated. The thermal resistance of the GaAs TLM patterns formed on the diamond and sapphire substrates was determined to be 6 and 34.9 K/W, respectively. The GaAs TLM patterns formed on the diamond showed an excellent heat dissipation property due to the high thermal conductivity of diamond.

### 1. Introduction

GaAs-based compound semiconductors have been extensively used to fabricate high-power and high-frequency devices, such as field-effect transistors (FETs), high electron mobility transistors (HEMTs), heterojunction bipolar transistors (HBTs), and laser diodes [1–4]. Such devices will produce a large amount of heat by self-heating that needs to be spread out through GaAs substrate, especially for the HEMTs and laser diodes. The thermal conductivity of GaAs (0.54 W/cm·K) is very low, which is almost one-third that of Si (1.51 W/cm·K). Therefore, the heat will be concentrated in a few discrete locations within sub-micron length scales and result in an increase in the device temperature, which will severely limit the reliability and performance of the devices. The important parameters of the devices, such as gain, saturated power, and maximum frequency are highly dependent upon the thermal management of the devices [5,6]. Therefore, the substrate with high thermal conductivity and high insulation property is very important to achieve

low dielectric loss and high heat dissipation performance of power devices.

In order to avoid rise in temperature of laser diodes, GaAs laser diode bonded to SiC substrate using surface activated bonding (SAB) method has been reported [7]. The simulated thermal resistance of GaAs/SiC bonded sample is relatively low compared to laser diode on GaAs and Si substrates. However, the thermal resistance is more than four times higher than that of laser diode on diamond. Diamond has the highest thermal conductivity of 18–22 W/cm·K and is one of the most potential materials to suppress the rise in the device temperature [8,9]. The integration of the GaAs-based device and diamond will be a more promising approach. However, the crystal structure of GaAs is different from that of the diamond, GaAs has a zinc blende structure, while diamond has a cubic structure. Furthermore, there is a large mismatch between the thermal expansion coefficients and lattice constants of GaAs and diamond. Thus, the direct growth of GaAs on the diamond is quite difficult and vice versa. An alternative approach is to directly integrate

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GaAs and diamond at room temperature. The GaAs film bonded to diamond by hydrophilic bonding method without post annealing process has been reported [10,11]. However, the fact that the oxide layer formed at the bonding interface will significantly degrade the thermal diffusion property across the interface, the hydrophilic bonding strength highly depends on the post annealing process temperature that means the bonding strength of the interface without annealing cannot fulfill requirement in terms of mechanical strength in devices fabrication process.

The room temperature bonding of diamond and GaN using a silicon amorphous layer by SAB method has been demonstrated [12]. However, it is difficult to withstand the annealing process higher than 700 °C during the GaN-based power device manufacturing process. Because the silicon amorphous layer will be recrystallized by the high temperature annealing process, and the recrystallized Si layer has a large mismatch with the thermal expansion coefficient of diamond and GaN, which will cause peeling of the bonding interface. Recently, T. Matsumae et al. demonstrated the direct bonding of diamond and Ga<sub>2</sub>O<sub>3</sub> under atmospheric conditions using OH-terminated method by oxygen plasma irradiation and H<sub>2</sub>SO<sub>4</sub>/H<sub>2</sub>O<sub>2</sub> cleaning [13]. The bonding area was very small, and some cracks were observed in the Ga<sub>2</sub>O<sub>3</sub> bonded to diamond, which makes it difficult to apply to device applications. The direct bonding of Si and diamond using SAB method has been reported [14]. More importantly, the SAB-fabricated Si/diamond interface demonstrated extremely high thermal stability (up to 1000 °C) and high applicability [15,16]. However, the only flaw is that there was a thick amorphous carbon layer formed at the bonding interface due to the Ar fast atom beam (FAB) irradiation in the surface activation process, which will largely degrade the interfacial physical property and mechanical strength. Therefore, it is a challenge to achieve a GaAs/diamond heterointerface with no amorphous carbon layer for applying to high power devices.

In this work, we explore the direct bonding of GaAs and diamond without forming amorphous carbon layer at room temperature using SAB. The structure and the atomic behavior of the GaAs/diamond bonding interface are investigated by scanning transmission electron microscopy (STEM) and energy-dispersive X-ray spectroscopy (EDX). The thermal stability of the bonding interface is tested at 400 °C in N<sub>2</sub> gas ambient pressure, which is necessary during GaAs devices fabrication process. The fabrication of the transmission line model (TLM) patterns on the GaAs layer bonded to diamond is demonstrated. The thermal dissipation characteristics of the TLM patterns formed on the GaAs layer bonded to diamond are investigated by a thermal graphic camera observation under applied power.

## 2. Experimental methods

A high-pressure and high-temperature synthetic Ib type (100) single crystal diamond substrate and a GaAs/InGaP epitaxial substrate were bonded to each other through SAB at room temperature [17–19]. The GaAs/InGaP epitaxial substrate was composed of a 200-nm-thick GaAs and a 100-nm-thick InGaP etch-stopper grown on a GaAs (100) substrate. Before bonding, the diamond bonding surface was polished by chemical mechanical polishing (CMP) and cleaned with the SPM (H<sub>2</sub>SO<sub>4</sub>: H<sub>2</sub>O<sub>2</sub> = 4:1) at 80 °C for 10 min, then rinsed with deionized water for 3 min, dried under N<sub>2</sub> flow. The GaAs/InGaP epitaxial substrate was cleaned with acetone and isopropyl alcohol in an ultrasonic bath for 300 s, dried under N<sub>2</sub> flow. After cleaning, the diamond and GaAs/InGaP epitaxial substrates were set in the SAB facility for direct bonding. The surfaces of the diamond and GaAs were simultaneously activated by the Ar FAB irradiation with a power of 1.6 kV and 1.6 mA for 240 s under a background vacuum pressure of  $5.0 \times 10^{-7}$  Pa. After the surface activation, the irradiated surfaces of diamond and GaAs were brought into contact by applying a pressure of 5 GPa for 60 s at room temperature. After bonding, the GaAs substrate and InGaP layer were removed by mechanical polishing and selective wet etching to obtain a

200-nm-thick GaAs layer bonded on diamond substrates. Optical microscope images of the bonded sample and the GaAs layer bonded to the diamond after removing the GaAs substrate and InGaP etch-stopper layer are shown in Fig. 1(a) and (b), respectively. A partially unbonded area was observed, which is due to the adhesion of some contaminations to the surface before bonding. After removing GaAs substrate and InGaP layer, an about 20% reduction in the bonding area was confirmed, which is due to the removal process of the GaAs substrate and InGaP layer. TLM patterns of AuZn/Ti/Au multilayers were fabricated on the GaAs layer bonded to diamond by photolithography and

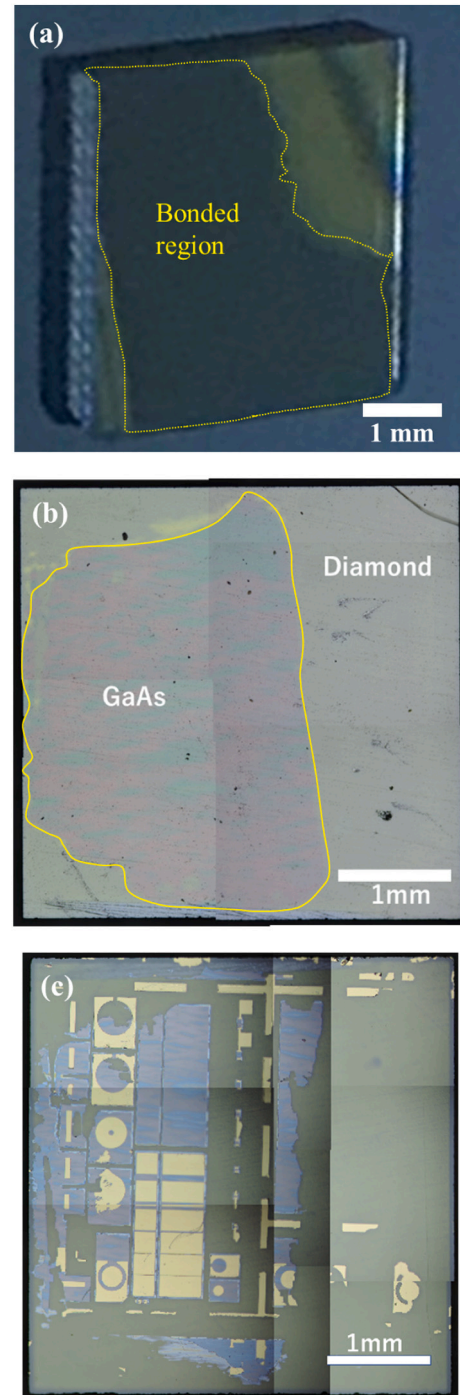


Fig. 1. Optical microscope images of the GaAs/diamond bonded sample surface (a), the GaAs thin layer bonded to the diamond after removing GaAs substrate and InGaP etch-stopper layer (b), and the TLM patterns fabricated on GaAs layer bonded to diamond.

evaporating processes, as shown in Fig. 1(b). Besides, the TLM pattern with the same structure was also fabricated on the GaAs layer bonded to the sapphire substrate that was used as a reference.

The morphology of the diamond surface before and after Ar fast atom beam (FAB) irradiation during the bonding process was investigated by atomic force microscopy (AFM: SPM-9600) with a vertical resolution of 0.01 nm. The GaAs/diamond bonded sample was annealed at 400 °C for 5 min in N<sub>2</sub> gas ambient pressure. A heating rate of 50 °C/min was conducted and the bonded sample was cooled down naturally after finishing the annealing process. The nanostructure of the GaAs/diamond bonding interface without and with annealing at 400 °C was examined by TEM, high-angle annular dark-field (HAADF), and energy-dispersive x-ray spectroscopy (EDX) under STEM with a JEOL JEM-ARM200F analytical microscope. The TEM samples were fabricated using the focused ion beam (FIB) technique (Helios NanoLab600i; Thermo Fisher Scientific). The surface temperature distribution of the GaAs TLM patterns was characterized by an infrared (IR) thermography camera (ViewOhre Imaging MCR32-XA0350-3×) at different applied powers.

### 3. Results

The Nomarski microscope image of the diamond surface is shown in Fig. 2(a). Some damages and dents are observed on the surface. The damage should be caused during the mechanical polishing of the bonding surface. The AFM images of the diamond surface before and after Ar FAB irradiation during the bonding process are shown in Fig. 2 (b) and (c), respectively. The root mean square (RMS) values of the surface roughness before and after Ar FAB irradiation were measured to be 0.05 and 0.07 nm, respectively. The RMS value of the surface roughness after irradiation seemed to slightly increase. However, such difference is in the range of the measurement error. A nano-level flat surface was obtained by the CMP process and the surface roughness was not affected by Ar FAB irradiation. Nano-level surface roughness is a critical factor for dissimilar material direct bonding at room temperature.

Fig. 3(a), (b), and (c) show a cross-sectional TEM and HAADF-STEM images and an X-ray intensity profile of C, Ga, As, Fe atoms across the bonding interface without annealing, respectively. The microstructure of the bonding interface is quite sharp and clear. No nano-voids and cracks were observed at the interface, which indicates that the GaAs are very closely bonded with the diamond. There is an intermediate layer formed at the GaAs/diamond bonding interface, the thickness of the intermediate layer was estimated to be about 2 nm. Some coherent lattice fringes of GaAs and diamonds were observed in the intermediate layer, which indicates that the intermediate layer is a crystal defect layer composed of diamond and GaAs. The HAADF-STEM image shows that the intermediate layer is mainly composed of the C atom.

The density gradients of Ga, As, C atoms were observed in the X-ray intensity profile of the interface, which indicated that there is an atomic intermixing layer formed at the bonding interface. The Fe atoms were intentionally induced into the bonding interface during the Ar FAB irradiation process to accurately determine the location of the bonding interface. A small peak of Fe atom was also observed in the X-ray intensity profile. The Fe atom should be located on the activated surface after the Ar FAB. Therefore, the density of the Fe atom is the maximum in the bonding interface. Based on such a hypothesis, we conclude that the peak location of the Fe atom is the bonding interface. The thickness of the GaAs and diamond crystal defect layers can be estimated to be about 0.4 and 1.6 nm, respectively.

Fig. 4(a) and (b) show a low and high magnification cross-sectional TEM images of the GaAs/diamond interface with annealing at 400 °C, respectively. No debonding regions caused by the difference in thermal expansion coefficient of GaAs and diamond was observed at the bonding interface, as shown in Fig. 4(a). Like the bonding interface without annealing, a crystal defect layer was also observed at the interface, no changes were observed in the thickness and interfacial structure. In

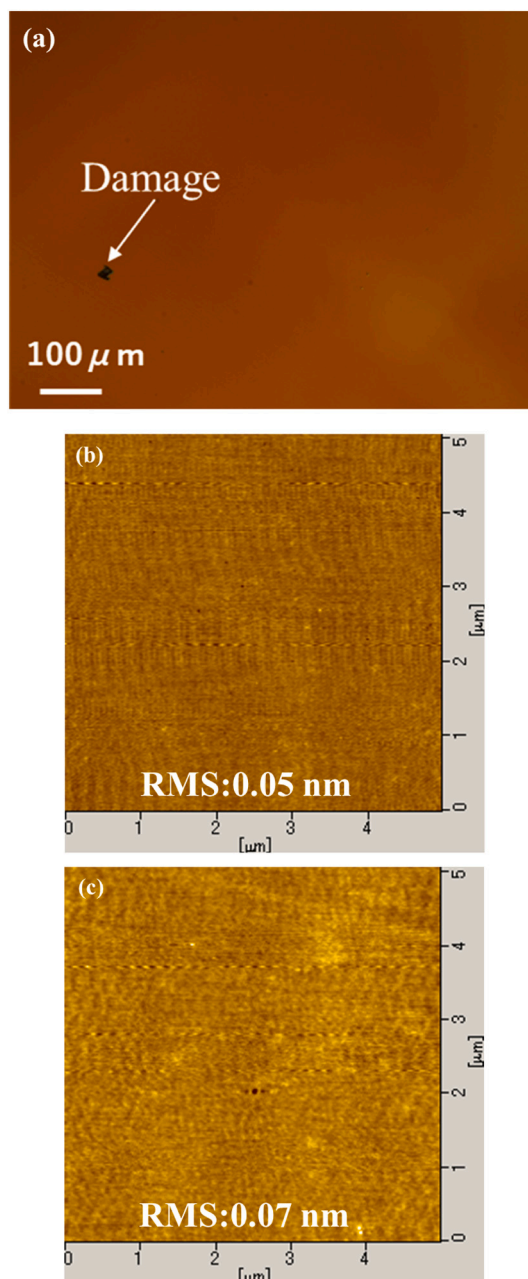


Fig. 2. Nomarski microscope image of diamond surface (a) and AFM images of diamond surfaces before (b) and after (c) Ar FAB irradiation.

addition, no atomic density distribution changes (not shown) were observed in the X-ray intensity profile of the interface.

The top view images and IR thermography images of the TLM patterns fabricated on GaAs layer bonded to diamond and sapphire substrates at an applied power of 0.4 W and the applied power dependence of the temperature rise for the GaAs TLM patterns formed on the diamond and sapphire substrate are shown in Fig. 5(a) and (b), (c) and (d), and (e), respectively. Before applying power, the surface temperature of the GaAs TLM patterns was measured to be 33 °C. When a power of 0.4 W was applied, the surface temperature of the GaAs TLM pattern formed on the diamond substrate increased to 36 °C (temperature rise  $\Delta$  3 °C), while the temperature of the GaAs TLM pattern formed on the sapphire substrate increased to 47 °C (temperature rise  $\Delta$  14 °C). The temperature rise of the GaAs TLM patterns is proportional to the applied power. The thermal resistance value of the GaAs TLM patterns formed on the diamond and sapphire substrates was extracted to be 6 and 34.9 K/W,



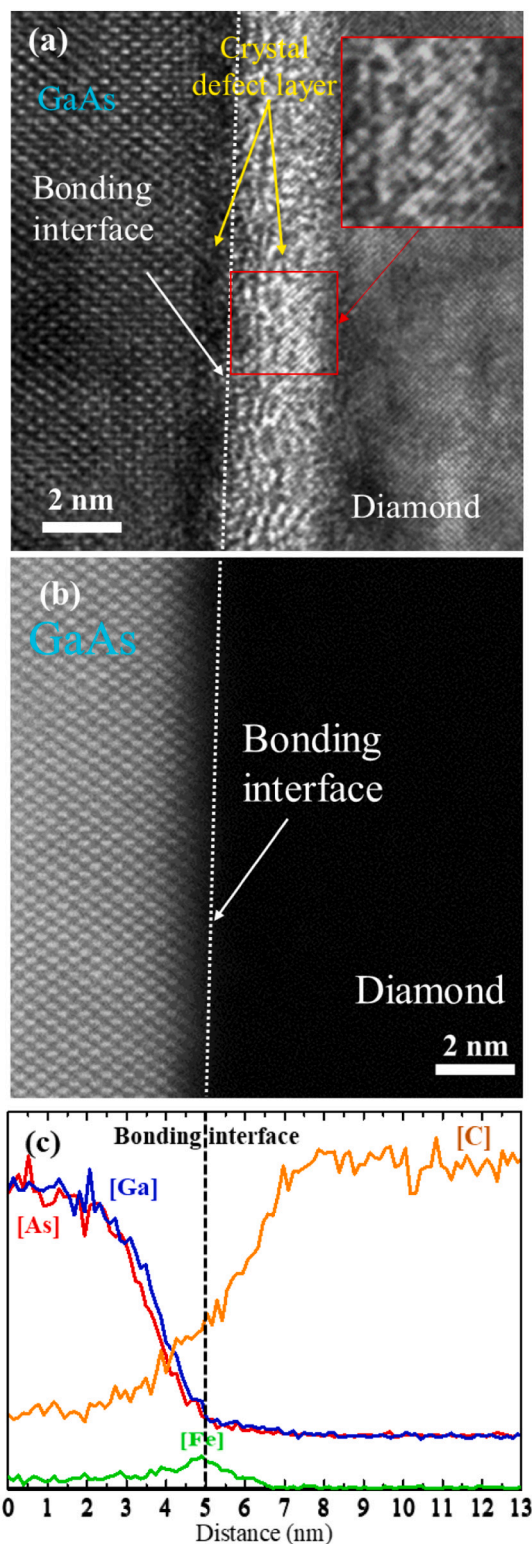


Fig. 3. A cross-sectional TEM (a) and HAADF-STEM (b) images of the GaAs/diamond bonding interface without annealing and X-ray intensity profiles of C, Ga, As, Ar, Fe in the bonding interface (c).

respectively. The thermal resistance value of the GaAs TLM patterns formed on the diamond was about one fifth of that on the sapphire substrate.

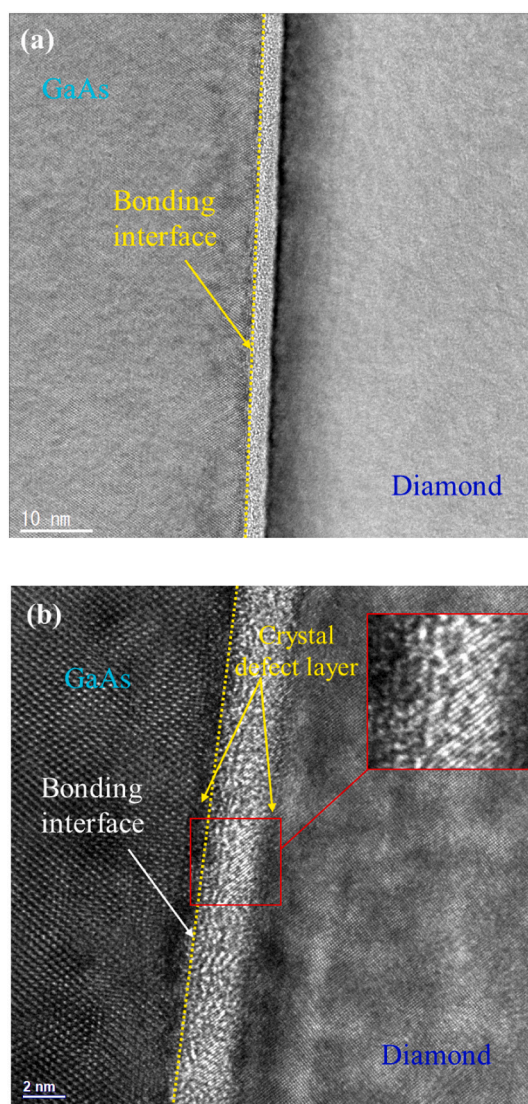


Fig. 4. A low (a) and high (b) magnification cross-sectional TEM images of the GaAs/diamond bonding interface with annealing at 400 °C.

#### 4. Discussion

The crystal defect layer formed at the GaAs/diamond bonding interface is unlike the previous reports that there was an amorphous layer formed at the Si/Si [20], Si/GaAs [21], Ge/Ge [22], and Si/SiC [23] interfaces fabricated by SAB. On the other hand, a crystal defect layer formed at the GaAs/GaAs interface fabricated by SAB has been reported [24]. Besides, it has also been reported that a-GaAs crystal defect layer and a-Si amorphous layer were both observed at the SAB-fabricated GaAs/Si interface [25]. An about 20% reduction of the As atom density was occurred in the GaAs crystal defect layer of the interface. It is most important to note that the diamond crystal defect layer formed at the GaAs/diamond bonding interface is in large contrast to that for the SAB-fabricated Si/diamond interface [14], where an amorphous carbon layer with a thickness of about 20 nm formed at the interface has been reported, due to the Ar FAB excess irradiation on the diamond surface during the bonding process. No amorphous carbon layer was formed at the GaAs/diamond bonding interface due to the lowered Ar FAB irradiation energy on the diamond surface impact. Meanwhile, these results indicate that the formation of the amorphous layer or the crystal defect layer at the bonding interface can be controlled by changing the Ar FAB irradiation energy.

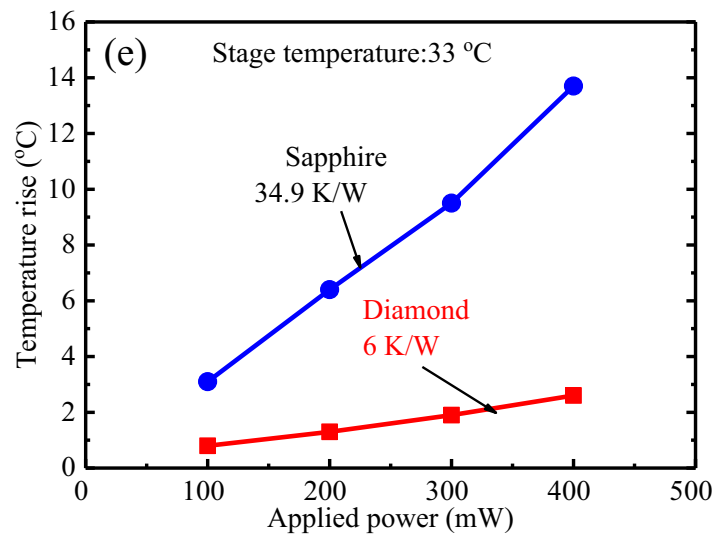
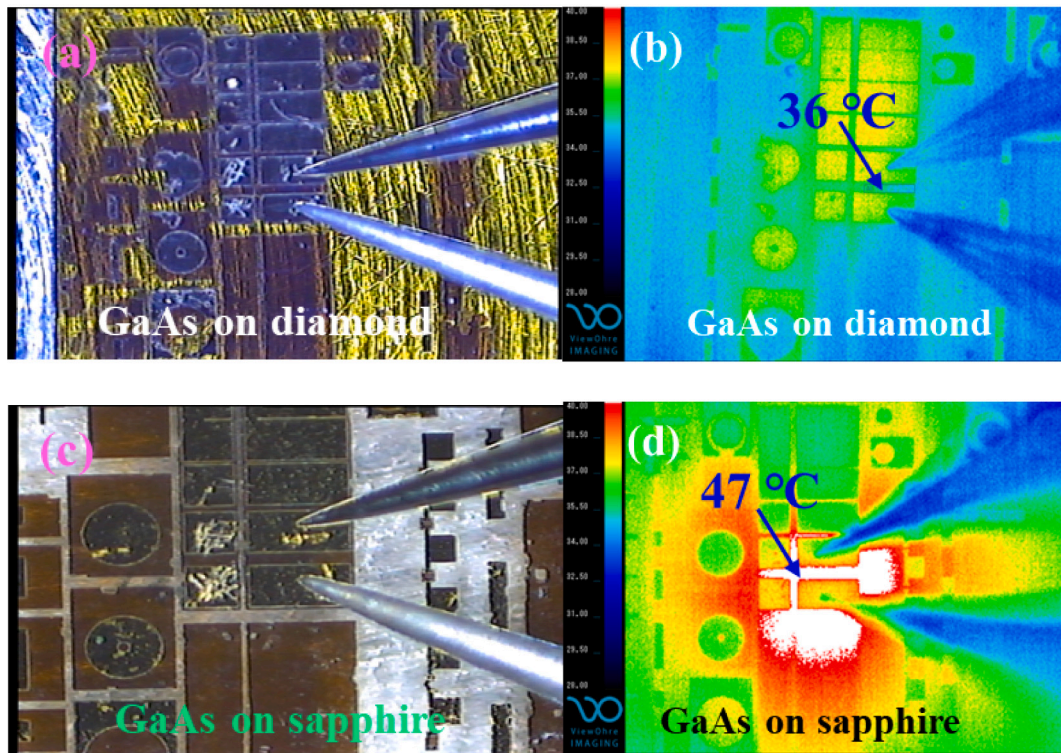


Fig. 5. A top view image and IR thermography image of the GaAs TLM patterns formed on the diamond (a) (b) and sapphire (c) (d) substrates at 0.4 W and the applied power dependence of the temperature rise for the GaAs TLM patterns formed on the diamond and sapphire substrates (e).

A similar crystal defect layer formed at the Ga<sub>2</sub>O<sub>3</sub>/diamond interface fabricated by OH-terminated method has been reported [13]. However, the Ga<sub>2</sub>O<sub>3</sub>/diamond interface is very difficult to withstand the high temperature annealing process required for device fabrication processes. Because some cracks were observed in the Ga<sub>2</sub>O<sub>3</sub> bonded to diamond during the bonding process at as low as 70 °C. No interfacial debonding was observed at the interface after annealing at 400 °C, which indicated that the GaAs/diamond bonding interface has a good thermal stability and is strong enough to withstand device fabrication processing. The bonding interface with high thermal stability was contributed to the atomic intermixing layer formed at the bonding interface that played a role of relaxing thermal stress caused by the difference in thermal expansion coefficients between diamond and Si. Similar results have been found at Si/diamond interface fabricated by SAB [16].

The heat of the GaAs TLM pattern is mainly generated in the active region and spreads out down to the substrate. The thermal resistance of the GaAs TLM pattern is the sum of the thermal resistance of the GaAs layer and the diamond or sapphire substrate, which could be calculated using the following equations [26]:

$$R_{th} = \frac{1}{2 \cdot k \cdot (x - y) \cdot \tan\theta} \cdot \ln \frac{x \cdot (y + 2 \cdot t \cdot \tan\theta)}{y \cdot (x + 2 \cdot t \cdot \tan\theta)}$$

where  $t$  and  $\kappa$ ,  $x$  and  $y$ , and  $\theta$  are the thickness and thermal conductivity of the substrate, the width and length of the TLM pattern, and the heat downward spreading angle, respectively. Here, we assume that the  $\theta$  is 45° [26,27], the heat flux is constant at respective layer, the thermal resistance of the bonding interface and the thermal resistance between the substrate and the heat sink are ignorable, and the substrate backside



temperature is same as that of the heat sink. The thickness and  $\kappa$  values of the GaAs layer, the diamond substrate, and the sapphire substrate are 0.2 and 0.5, 500 and 20, and 370  $\mu\text{m}$  and 0.42 W/cm $\cdot$ K, respectively. The heat source is an electrode-electrode region with  $x = 400 \mu\text{m}$  and  $y = 60 \mu\text{m}$ . For the substrate, the  $x$  and  $y$  values are  $x_{\text{substrate}} = x_{\text{GaAs layer}} + 2t_{\text{GaAs layer}} \tan \theta$  and  $y_{\text{substrate}} = y_{\text{GaAs layer}} + 2t_{\text{GaAs layer}} \tan \theta$ , respectively, to take heat spreading into account.

The thermal resistances of the GaAs layer and the diamond and sapphire substrates were calculated to be 0.17, 1.19, and 53.83 K/W, respectively. Thus, the total thermal resistance of the GaAs TLM pattern formed on the diamond and sapphire substrates is 1.36 and 54 K/W, respectively, which is mainly determined by the thermal resistance of the diamond and sapphire substrates. The calculated thermal resistance value of the GaAs TLM pattern formed on the diamond substrate is smaller in comparison with the experimental value in Fig. 5(e). Nevertheless, the calculated value of the GaAs TLM pattern formed on the sapphire substrate is larger than the experimental value. Such discrepancy should be due to a large thermal resistance between diamond and the heat sink and a large surface heat dissipation area of the GaAs TLM pattern formed on the sapphire substrate.

For the IR thermography measurement, the GaAs TLM patterns formed on the diamond and sapphire substrates were directly put on the heat sink without solder bonding. Therefore, a large thermal resistance is existing between the diamond or sapphire and the heat sink. Meanwhile, since the thermal resistance (53.83 K/W) of the sapphire substrate itself is very high, the thermal resistance of the interface and the thermal resistance between the sapphire and the heat sink can be ignored. However, the thermal resistance between the diamond and the heat sink will be a large thermal barrier for heat transfer from the diamond to the heat sink due to the low thermal resistance value of the diamond substrate. These results indicate that a large discrepancy between the calculated value and the experimental value in the thermal resistance of the GaAs TLM patterns formed on the diamond should be mainly due to the thermal resistance between the diamond and the heat sink.

For the thermal resistance of the GaAs/diamond bonding interface, a small interfacial thermal resistance value can be expected due to the low crystal defect bonding interface. A small interfacial thermal resistance value obtained at the low crystal defect Cu/diamond interface fabricated by SAB has been reported [28]. On the other hand, a large thermal resistance should be existed at the SAB-fabricated GaN/diamond interface with a silicon amorphous layer [12]. Since the thermal conductivity of the silicon amorphous layer is as low as 1.8 W/m $\cdot$ K. Similarly, the amorphous layer formed at the GaAs/SiC interface fabricated by SAB method will largely degrade the thermal conductive properties of the interface [11]. By contrast, the GaAs/diamond bonding interface is more significant in terms of heat dissipation. Therefore, to improve the heat dissipation characteristics of power devices, it is necessary to employ high thermal conductivity substrate and form high-quality interface.

A large area temperature distribution was observed on the surface of the GaAs TLM pattern formed on the sapphire substrate as shown in Fig. 5(d). This result indicates that the heat in the GaAs TLM patterns on the sapphire substrate is diffused toward the horizontal direction due to GaAs has more excellent thermal conductivity compared with sapphire. A part heat generated in the GaAs TLM pattern was dissipated through the surface contacting with air, which induced the discrepancy between the experimental value and the calculated value of the thermal resistance. From these results, we confirmed that a high-quality GaAs/diamond heterointerface can be achieved and diamond is a very excellent substrate for reducing the thermal resistance of the devices to realize high power operation.

## 5. Conclusions

We demonstrated the fabrication of the GaAs/diamond bonding interface and the thermal characteristics of the GaAs TLM patterns

formed on the diamond substrate. A GaAs and diamond crystal defect layer with a thickness of about 0.4 and 1.6 nm, respectively, was formed at the bonding interface. No interfacial debonding and cracks were observed at the interface after annealing at 400  $^{\circ}\text{C}$ . The GaAs TLM patterns formed on the diamond revealed extremely low thermal resistance compared with that of the GaAs TLM patterns formed on the sapphire substrate, which was contributed to the high thermal conductivity of the diamond substrate.

## CRedit authorship contribution statement

**Jianbo Liang:** conceptualization, Formal analysis, **Yuji Nakamura:** the sample fabrication, **Tianzhuo Zhan:** Formal analysis, **Yutaka Ohno:** TEM analysis, **Yasuo Shimizu:** TEM sample fabrication, **Kazu Katayama:** Formal analysis, **Takanobu Watanabe:** Formal analysis, **Hideto Yoshida:** TEM analysis, **Yasuyoshi Nagai:** EDS analysis, **Hongxing Wang:** Investigation, **Makoto Kasu:** Formal analysis, and **Nao-teru Shigekawa:** Formal analysis.

## Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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